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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,809	12/31/2001	Ge Nong	01-HK-048 (STM101-01048)	5323
7590 Lisa K. Jorgenson STMicroelectronics, Inc. 1310 Electronics Drive Carrollton, TX 75006				
04/13/2010				
EXAMINER				
MURPHY, RHONDA L				
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2462				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/036,809

**Applicant(s)**

NONG, GE

**Examiner**

RHONDA MURPHY

**Art Unit**

2462

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 January 2010.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-20 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 04 January 2010 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO/GS/US)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. This office action is responsive to the communication filed on 1/4/10. Accordingly, claims 1-20 are currently pending.

### ***Response to Arguments***

1. Applicant's arguments filed 1/4/10 have been fully considered but they are not persuasive. Applicant argues the prior art of record does not teach the amended limitations "*configured to receive at least one incoming fixed data packet at a first data rate and further configured to output said at least one incoming fixed data packet at a second data rate, wherein the second data rate is at least twice the first data rate and is configured to promote an emulated buffered crossbar., wherein the queuing of the input buffer is performed through a virtual output queue where the incoming fixed data packets are queued according to their destination port" and an "emulated crossbar."* However, Examiner respectfully disagrees and would like to direct the Applicant to the rejection below. Applicant further argues "there is no reference in Krishna to using the "Arbiter" of Krishna to an "emulated buffered crossbar." In order to further clarify the scheduling controller, the Applicant has also added the element that the scheduling controller promotes an emulated buffered crossbar." Krishna does disclose using the arbiter to emulate a buffered crossbar in column 7, lines 57 to column 8, line 4, which recites in part, "*By having a one-to-one correspondence between the number of virtual output queues and the number of output ports, each virtual output queue 56, 57 and 58 is able to buffer the cells that must be transmitted to that virtual output queue's*

*corresponding output port, either 59, 60 or 61, respectively. **The process of receiving and queuing cells into the virtual output queues 56, 57 and 58 of each input port 50, 51 and 52 is the input buffering portion of network device processing.** Once the cells are buffered or queued in the virtual output queues, they are ready for transfer to their respective output ports. The operation of cell transfers in network device 49 is controlled by the arbiter 90."* Krishna further describes the first and second data rates in column 8, lines 10-15 and 34-38.

2. In addition, Applicant submits that the prior art of record does not teach the scheduling controller "connected to the bufferless, non-blocking interconnecting network wherein..., the scheduling controller controls the configuration of the bufferless, non-blocking interconnecting network. Applicant argues the arbiter (90) is not connected to the switch fabric (89) such that it can control the configuration of the switch fabric, and states the arbiter (90), is connected to the input ports and output ports. Examiner agrees the arbiter is connected to the input and output ports. However, the arbiter is also connected to the switch fabric/crossbar 89 via the input and output ports and Krishna describes the arbiter controlling the configuration of the switch fabric/crossbar 89 (bufferless, non-blocking interconnecting network) by way of the input/output ports. For example, Krishna teaches a scheduling controller (arbiter 90) connected to the bufferless, non-blocking interconnecting network as illustrated in Figure 1; column 1, lines 22-30 and further described in column 5, lines 8-13. Examiner would like to direct the applicant's attention to figure 1, crossbar 89 and col. 3, lines 63-65 and also col. 6, lines 60-61, in which channels 80-88 form crossbar 89, which does not include any

buffers. Thus, producing a *bufferless, non-blocking interconnecting network*.

Furthermore, Krishna teaches the scheduling controller (arbiter 90) controls the configuration of the bufferless, non-blocking interconnecting network in column 1, lines 22-30, which recites "*The internal switching fabric of a network device interconnects input ports to output ports and is typically controlled by an arbiter. The arbiter typically controls the flow of data from input to output ports, using an arbitration algorithm to sequentially make matches between the ports. The switching fabric then uses the matches to transfer the data once no more matches can be made. **The process of an arbiter controlling a switch fabric to interconnect input and output ports is referred to as "switching" the data.***" Thus, the arbiter 90 is connected to the crossbar/switch fabric 89 and this is further described in col. 8, lines 34-38.

3. Therefore, it is Examiner's position that all claim limitations have been met and the rejection has been maintained.

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1- 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishna et al. (US 6,563,837).

**Regarding claim 1**, Krishna teaches a network device (Fig. 1; device 49) comprising: N input buffers (queues 56, 57, 58) configured to receive at least one incoming fixed data packet at a first data rate (col. 8, lines 34-35) and further configured to output said at least one incoming fixed data packet at a second data rate (col. 8, lines 34-38), wherein the second data rate is at least twice the first data rate (col. 8, lines 37-38) and is selected to promote an emulated buffered crossbar (col. 7, line 57 to col. 8, line 4), and wherein the queuing of the input buffer is performed through a virtual output queue such with incoming fixed data packets queued according to their destination port (col. 7, line 57 to col. 8, line 4);

N output buffers (queues 65) configured to receive fixed-size data packets at said second data rate (col. 8, lines 10-15, 34-38) and configured to output said fixed-sized data packets to an output port (62) at said first data rate (col. 9, lines 6-9), wherein said N output buffers are internal to said switch fabric (see Fig. 1) and are external to said output port (see Fig. 1);

and a bufferless, non-blocking interconnecting network (Fig. 1, col. 3, lines 63-65; col. 6, lines 60-61; channels 80 – 88 form crossbar 89, which does not include any buffers) configured to receive from said N input buffers said fixed-size data packets at said second data rate and configured to transfer said fixed-size data packets to said N output buffers at said second data rate (col. 8, lines 10-15, 34-38) and

a scheduling controller (arbiter 90) connected to the bufferless, non-blocking interconnecting network (see Fig. 1; col. 1, lines 22-30; further described in col. 5, lines 8-13), wherein the scheduling controller is configured to determine a maximal

configuration of the bufferless, non-blocking interconnecting network (col. 8, lines 5-10, 16-22) and emulated crossbar based upon the data in the N input buffers (col. 7, line 57 to col. 8, line 4) and controls the configuration of the bufferless, non-blocking interconnecting network through communications with the bufferless, non-blocking interconnecting network (col. 1, lines 22-30; further described in col. 8, lines 34-38).

Krishna fails to explicitly call the network device 49 a switch. However, the network device, which includes the fabric to switch data packets, functions as a switch.

Therefore, it would have been obvious to one skilled in the art to use Krishna's network device as a switch for switching the data packets through the network.

**Regarding claims 2 and 5**, Krishna teaches a bufferless, non-blocking interconnecting network, comprising a bufferless crossbar (Fig. 1, col. 3, lines 63-65; col. 6, lines 60-61; channels 80 – 88 form crossbar 89, which does not include any buffers).

**Regarding claims 3 and 6**, Krishna teaches each of said N input buffers is at least twice the size of each of said N output buffers (see Fig. 1).

**Regarding claim 4**, Krishna teaches the same limitations described above in the rejection of claim 1. Krishna further teaches wherein control of delay, jitter, throughput, and ordering of packets through the switch is controlled by the controller adjusting the emulated crossbar and through a virtual output queue (col. 1, lines 56-58; co. 7, lines 57-65; col. 8, lines 1-19; col. 15, lines 14-15).

**Regarding claims 7 and 14**, Krishna teaches a plurality of fixed-size data packet switches (all elements of Fig. 1, col. 7, lines 35-36), at least one of said fixed-size data packet switches comprising:

N input ports (Fig. 1; ports 53, 54, 55) configured to receive incoming fixed-size data packets at a first data rate and to output said fixed-size data packets at said first data rate (col. 8, lines 34-38);

N output ports (ports 62, 63, 64) configured to receive fixed-size data packets at said first data rate (col. 8, lines 10-15) and to output said fixed-sized data packets at said first data rate (col. 9, lines 6-9); and

a network device (device 49; col. 6, lines 60-61) interconnecting said N input ports and said N output ports (see Fig. 1) comprising:

N input buffers (queues 56, 57, 58) configured to receive incoming fixed-size data packets at a first data rate and to output said fixed-size data packets at a second data rate equal to at least twice said first data rate (col. 8, lines 34-38), wherein said N input buffers are internal to said network device (see Fig. 1) and are external to said N input ports (see Fig. 1) and are configured to queue the fixed-size data packets through a virtual output queue according to their destination port (col. 7, line 57 to col. 8, line 4);

N output buffers (queues 65) configured to receive fixed-size data packets at said second data rate (col. 8, lines 10-15, 34-38) and to output said fixed-sized data packets at said first data rate (col. 9, lines 6-9) wherein said N output buffers are internal to said switch fabric (see Fig. 1) and are external to said N output ports (see Fig. 1);

a bufferless, non-blocking interconnecting network (Fig. 1, col. 3, lines 63-65; col. 6, lines 60-61; channels 80 – 88 form crossbar 89, which does not



include any buffers) configured to receive from said N input buffers said fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N output buffers at said second data rate (col. 8, lines 10-15, 34-38); and

a scheduling controller (arbiter 90) connected to the bufferless, non-blocking interconnecting network (see Fig. 1; col. 1, lines 22-30; further described in col. 5, lines 8-13), wherein the scheduling controller is configured to emulate a crossbar within the bufferless, non-blocking interconnecting network (col. 7, line 57 to col. 8, line 4) and to determine a maximal configuration of the bufferless, non-blocking interconnecting network based upon the data in the N input buffers (col. 8, lines 5-10, 16-22) and controls the configuration of the bufferless, non-blocking interconnecting network (col. 1, lines 22-30; further described in col. 8, lines 34-38).

Krishna fails to explicitly call the network device 49 a switch. However, the network device, which includes the fabric to switch data packets, functions as a switch.

Therefore, it would have been obvious to one skilled in the art to use Krishna's network device as a switch for switching the data packets through the network.

**Regarding claims 8 and 15,** Krishna teaches a bufferless, non-blocking interconnecting network comprising a bufferless crossbar (Fig. 1, col. 3, lines 63-65; col. 6, lines 60-61; channels 80 – 88 form crossbar 89, which does not include any buffers).

**Regarding claims 9 and 16,** Krishna teaches each of said N input buffers is at least twice the size of each of said N output buffers (see Fig. 1).

**Regarding claims 10 and 17**, Krishna teaches a scheduling controller is configured to schedule transfer of said fixed-size data packets from said N input ports to said switch fabric (arbiter 90; col. 8, lines 24-38).

**Regarding claims 11 and 18**, Krishna teaches a scheduling controller is configured to schedule the transfer of said fixed-size data packets from said N output ports to an external device (col. 8, lines 5-15; 24-38).

**Regarding claims 12 and 19**, Krishna teaches a scheduling controller is configured to schedule the transfer of said fixed-size data packets from said N input buffers to said bufferless, non-blocking interconnecting network (col. 8, lines 5-15; 24-38).

**Regarding claims 13 and 20**, Krishna teaches a scheduling controller is configured to schedule the transfer of said fixed-size data packets from said N output buffers to said N output ports (col. 8, lines 5-15; 24-38).

### ***Conclusion***

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RHONDA MURPHY whose telephone number is (571)272-3185. The examiner can normally be reached on Monday - Friday 9:00 - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. M./  
Examiner, Art Unit 2462

/Donald L Mills/  
Primary Examiner, Art Unit 2462

